REMARKS

The Examiner objected to the drawings because the Examiner maintains the "integrated circuits elements constructed thereon [first surface of substrate], and extending a maximum distance...into said substrate," and "vias extending...greater than said maximum distance..." are not, according to the Examiner, shown in the drawings. Applicant respectfully disagrees.

The claimed element is a substrate having a first surface, "said first surface having a circuit layer comprising integrated circuit elements constructed thereon, and extending a maximum distance from said first surface into said substrate. Such layers are shown at 22, 32, and 42 in Figure 1 as well as in numerous other drawings. Such layers are conventional in the art, and hence, Applicant is free to show the element as a labeled representation as provided in 37 CFR 1.83(a). The layers are shown as rectangles having a finite depth with vertical lines that represent the circuit elements. It should also be noted that these drawings also show a number of vias, e.g. via 53, that extend from the surface of the substrate to a depth below the integrated circuit layer. Claims 1 and 7 have been amended to make it clear that the circuit layer having the integrated circuit elements extends the claimed distance into the substrate.

The Examiner rejected Claims 1-10 and 17 under U.S.C. 112, first paragraph. The Examiner maintains that there is no support for integrated circuit elements being constructed on the surface of the substrate and extending into the substrate. Applicant traverses this rejection. As noted above, the claimed element is a circuit layer that extends into the substrate and has circuit elements. The specification clearly shows such layers and discusses the layers including the fact that these layers are constructed using conventional integrated circuit fabrication techniques (See the discussion of Figure 1). Such layers have been conventional in the integrated circuit arts for over twenty years. Applicant is not aware of any requirement in the patent law that Applicant teach that which is widely known in the art.

Accordingly, Applicant submits that the drawings do not require any corrections, since the circuit layer in clearly shown in the drawings. Furthermore, the claims in question are not defective for lack of support because the claims are not supported in the specification.

I hereby certify that this paper is being sent by FAX to 703-872-9306.

Respectfully Submitted,

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